FPGA
[2]-FPGA.SchDoc

CPLD
[3]-CPLD.SchDoc

USB
[4]-USB.SchDoc

BeagleBlack Connectors
[5]-BeagleBlack Connectors.SchDoc

PMOD Connectors
[6]-PMOD Connectors.SchDoc

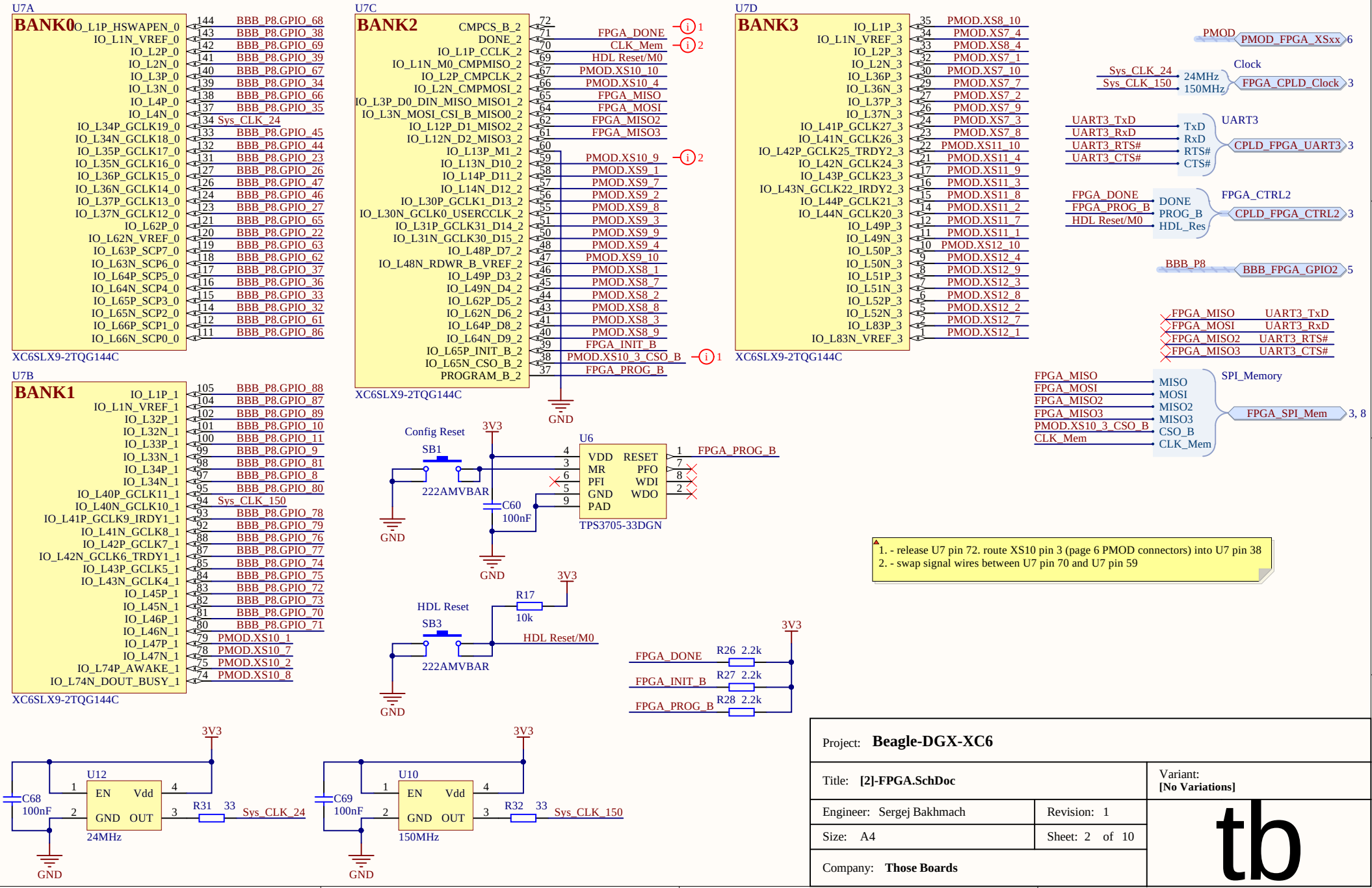
FPGA-Power
[7]-FPGA-Power.SchDoc

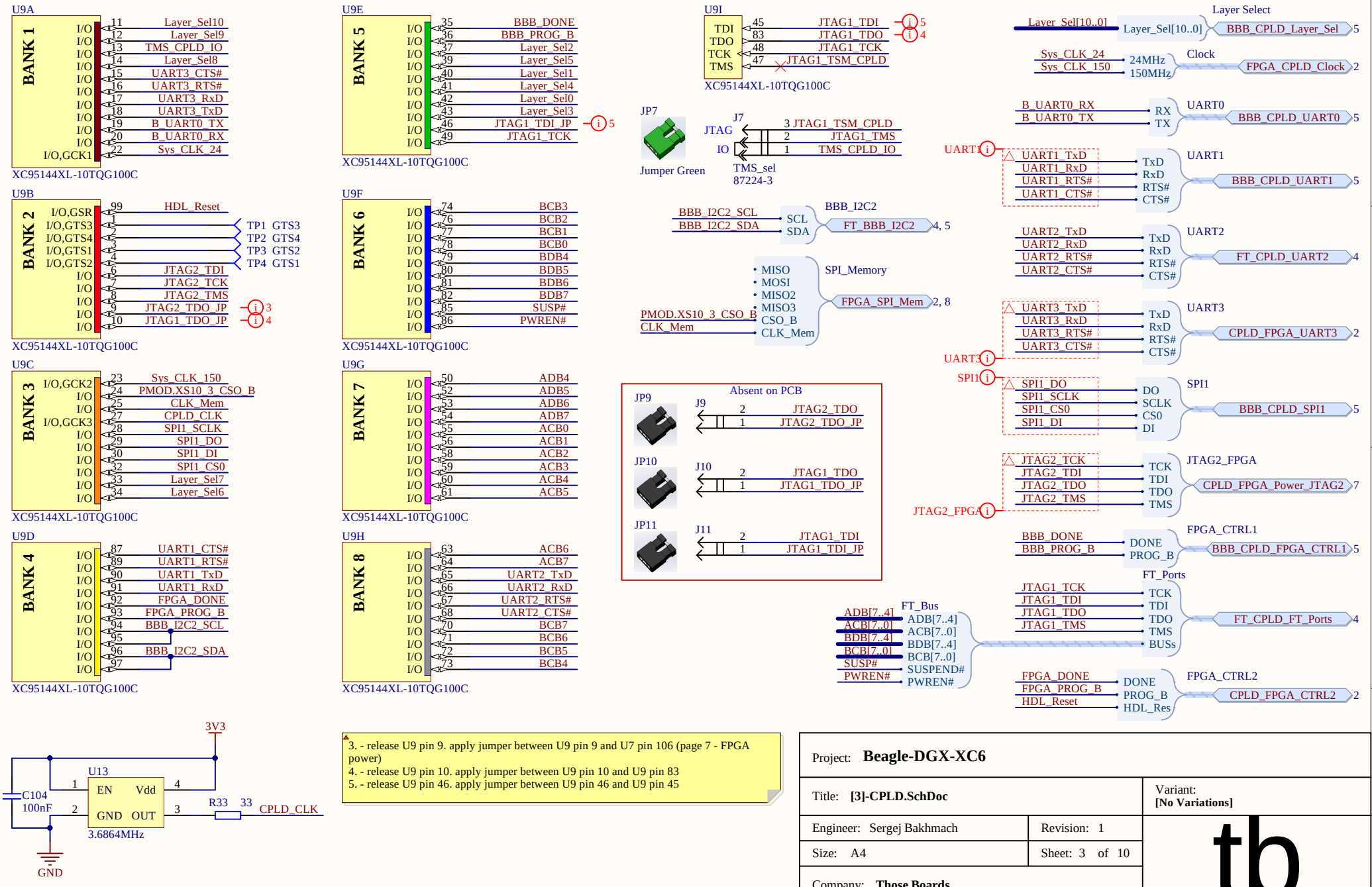
SPI_Memory
[8]-SPI_Memory.SchDoc

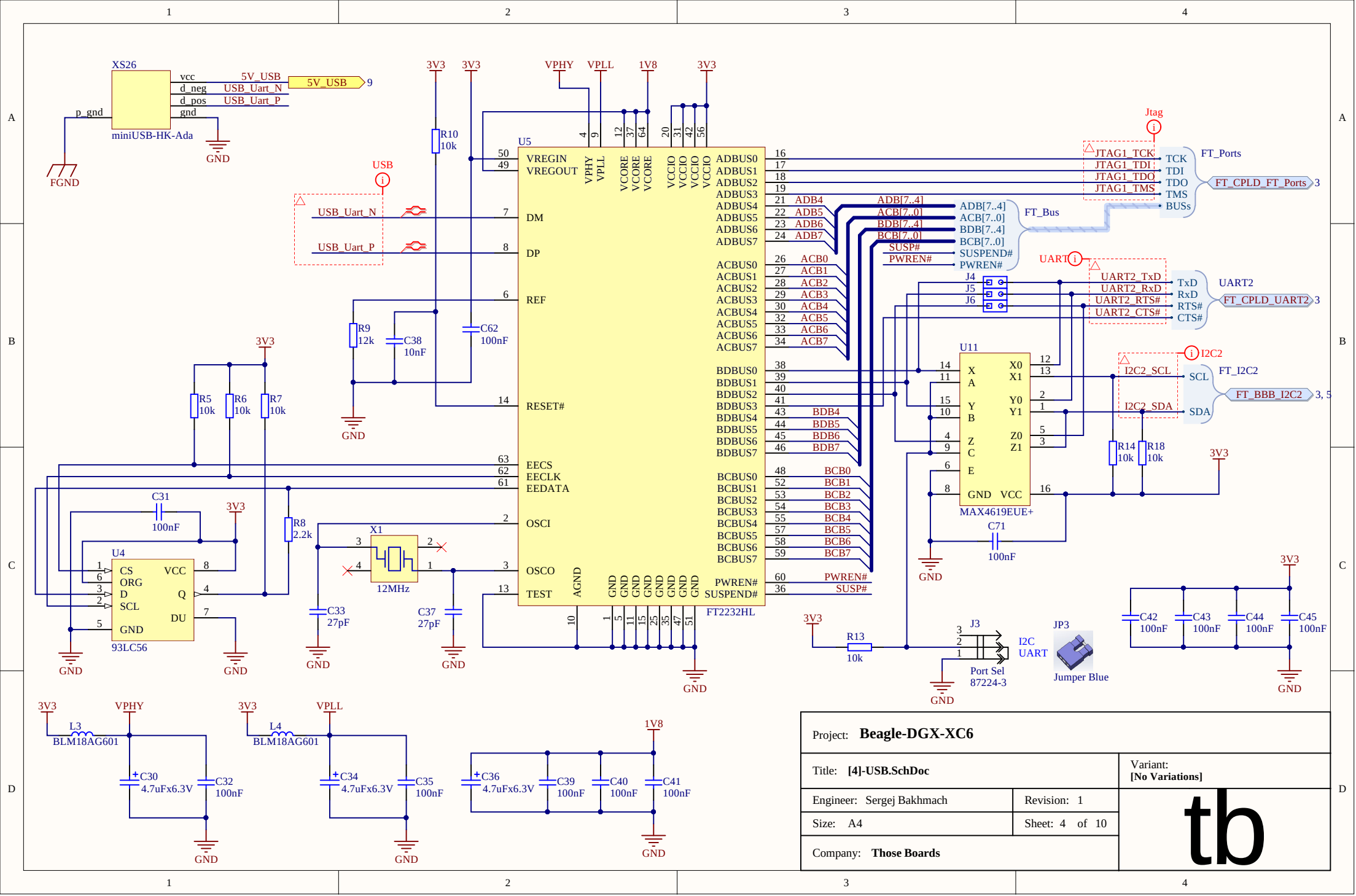
[9]-Power Supply
[9]-Power Supply.SchDoc

[10]-CPLD-Power
[10]-CPLD-Power.SchDoc

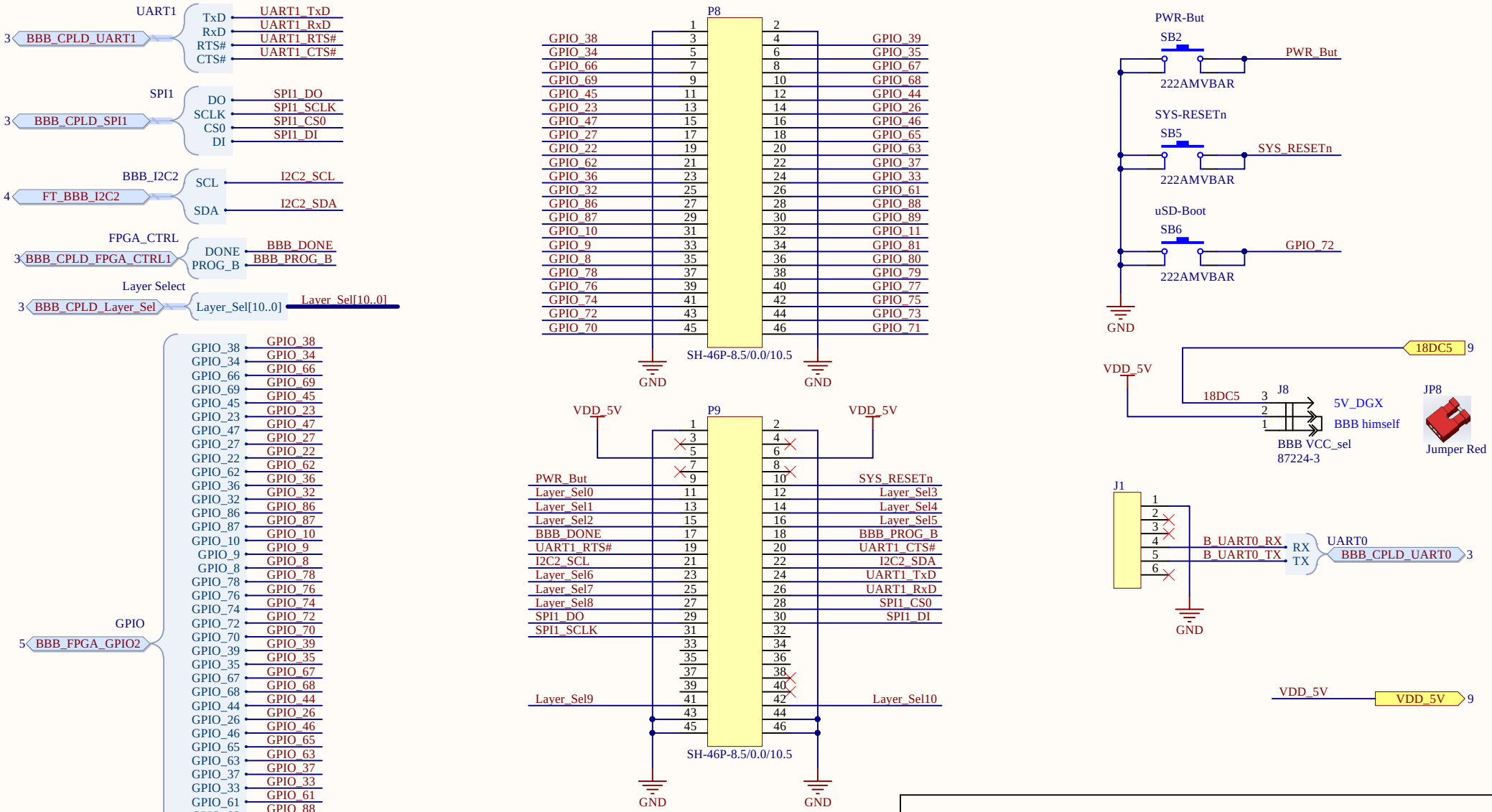
Project: **Beagle-DGX-XC6**		
Title: **[1]-Beagle-DGX-XC6 Top.SchDoc**		Variant: **[No Variations]**
Engineer: Sergej Bakhmach	Revision: 1	tb
Size: A4	Sheet: 1 of 10	
Company: **Those Boards**		


U7A
BANK0
IO_L1P_HSWAPEN_0 144 BBB_P8.GPIO_68
IO_L1N_VREF_0 143 BBB_P8.GPIO_38
IO_L2P_0 142 BBB_P8.GPIO_69
IO_L2N_0 141 BBB_P8.GPIO_39
IO_L3P_0 140 BBB_P8.GPIO_67
IO_L3N_0 139 BBB_P8.GPIO_34
IO_L4P_0 138 BBB_P8.GPIO_66
IO_L4N_0 137 BBB_P8.GPIO_35
IO_L34P_GCLK19_0 134 Sys_CLK_24
IO_L34N_GCLK18_0 133 BBB_P8.GPIO_45
IO_L35P_GCLK17_0 132 BBB_P8.GPIO_44
IO_L35N_GCLK16_0 131 BBB_P8.GPIO_23
IO_L36P_GCLK15_0 127 BBB_P8.GPIO_26
IO_L36N_GCLK14_0 126 BBB_P8.GPIO_47
IO_L37P_GCLK13_0 124 BBB_P8.GPIO_46
IO_L37N_GCLK12_0 123 BBB_P8.GPIO_27
IO_L62P_0 121 BBB_P8.GPIO_65
IO_L62N_VREF_0 120 BBB_P8.GPIO_22
IO_L63P_SCP7_0 119 BBB_P8.GPIO_63
IO_L63N_SCP6_0 118 BBB_P8.GPIO_62
IO_L64P_SCP5_0 117 BBB_P8.GPIO_37
IO_L64N_SCP4_0 116 BBB_P8.GPIO_36
IO_L65P_SCP3_0 115 BBB_P8.GPIO_33
IO_L65N_SCP2_0 114 BBB_P8.GPIO_32
IO_L66P_SCP1_0 112 BBB_P8.GPIO_61
IO_L66N_SCP0_0 111 BBB_P8.GPIO_86
XC6SLX9-2TQG144C
U7B
BANK1
IO_L1P_1 105 BBB_P8.GPIO_88
IO_L1N_VREF_1 104 BBB_P8.GPIO_87
IO_L32P_1 102 BBB_P8.GPIO_89
IO_L32N_1 101 BBB_P8.GPIO_10
IO_L33P_1 100 BBB_P8.GPIO_11
IO_L33N_1 99 BBB_P8.GPIO_9
IO_L34P_1 98 BBB_P8.GPIO_81
IO_L34N_1 97 BBB_P8.GPIO_8
IO_L40P_GCLK11_1 95 BBB_P8.GPIO_80
IO_L40N_GCLK10_1 94 Sys_CLK_150
IO_L41P_GCLK9_IRDY1_1 93 BBB_P8.GPIO_78
IO_L41N_GCLK8_1 92 BBB_P8.GPIO_79
IO_L42P_GCLK7_1 88 BBB_P8.GPIO_76
IO_L42N_GCLK6_TRDY1_1 87 BBB_P8.GPIO_77
IO_L43P_GCLK5_1 85 BBB_P8.GPIO_74
IO_L43N_GCLK4_1 84 BBB_P8.GPIO_75
IO_L45P_1 83 BBB_P8.GPIO_72
IO_L45N_1 82 BBB_P8.GPIO_73
IO_L46P_1 81 BBB_P8.GPIO_70
IO_L46N_1 80 BBB_P8.GPIO_71
IO_L47P_1 79 PMOD.XS10_1
IO_L47N_1 78 PMOD.XS10_7
IO_L74P_AWAKE_1 75 PMOD.XS10_2
IO_L74N_DOUT_BUSY_1 74 PMOD.XS10_8
XC6SLX9-2TQG144C
U7C
BANK2
CMPCS_B_2 72
DONE_2 71 FPGA_DONE
IO_L1P_CCLK_2 70 CLK_Mem
IO_L1N_M0_CMPMISO_2 69 HDL Reset/M0
IO_L2P_CMPCLK_2 67 PMOD.XS10_10
IO_L2N_CMPMOSI_2 66 PMOD.XS10_4
IO_L3P_D0_DIN_MISO_MISO1_2 65 FPGA_MISO
IO_L3N_MOSI_CSI_B_MISO0_2 64 FPGA_MOSI
IO_L12P_D1_MISO2_2 62 FPGA_MISO2
IO_L12N_D2_MISO3_2 61 FPGA_MISO3
IO_L13P_M1_2 60
IO_L13N_D10_2 59 PMOD.XS10_9
IO_L14P_D11_2 58 PMOD.XS9_1
IO_L14N_D12_2 57 PMOD.XS9_7
IO_L30P_GCLK1_D13_2 56 PMOD.XS9_2
IO_L30N_GCLK0_USERCCLK_2 55 PMOD.XS9_8
IO_L31P_GCLK31_D14_2 51 PMOD.XS9_3
IO_L31N_GCLK30_D15_2 50 PMOD.XS9_9
IO_L48P_D7_2 48 PMOD.XS9_4
IO_L48N_RDWR_B_VREF_2 47 PMOD.XS9_10
IO_L49P_D3_2 46 PMOD.XS8_1
IO_L49N_D4_2 45 PMOD.XS8_7
IO_L62P_D5_2 44 PMOD.XS8_2
IO_L62N_D6_2 43 PMOD.XS8_8
IO_L64P_D8_2 41 PMOD.XS8_3
IO_L64N_D9_2 40 PMOD.XS8_9
IO_L65P_INIT_B_2 39 FPGA_INIT_B
IO_L65N_CSO_B_2 38 PMOD.XS10_3_CSO_B
PROGRAM_B_2 37 FPGA_PROG_B
XC6SLX9-2TQG144C
U7D
BANK3
IO_L1P_3 35 PMOD.XS8_10
IO_L1N_VREF_3 34 PMOD.XS7_4
IO_L2P_3 33 PMOD.XS8_4
IO_L2N_3 32 PMOD.XS7_1
IO_L36P_3 30 PMOD.XS7_10
IO_L36N_3 29 PMOD.XS7_7
IO_L37P_3 27 PMOD.XS7_2
IO_L37N_3 26 PMOD.XS7_9
IO_L41P_GCLK27_3 24 PMOD.XS7_3
IO_L41N_GCLK26_3 23 PMOD.XS7_8
IO_L42P_GCLK25_TRDY2_3 22 PMOD.XS11_10
IO_L42N_GCLK24_3 21 PMOD.XS11_4
IO_L43P_GCLK23_3 17 PMOD.XS11_9
IO_L43N_GCLK22_IRDY2_3 16 PMOD.XS11_3
IO_L44P_GCLK21_3 15 PMOD.XS11_8
IO_L44N_GCLK20_3 14 PMOD.XS11_2
IO_L49P_3 12 PMOD.XS11_7
IO_L49N_3 11 PMOD.XS11_1
IO_L50P_3 10 PMOD.XS12_10
IO_L50N_3 9 PMOD.XS12_4
IO_L51P_3 8 PMOD.XS12_9
IO_L51N_3 7 PMOD.XS12_3
IO_L52P_3 6 PMOD.XS12_8
IO_L52N_3 5 PMOD.XS12_2
IO_L83P_3 2 PMOD.XS12_7
IO_L83N_VREF_3 1 PMOD.XS12_1
XC6SLX9-2TQG144C
PMOD
PMOD_FPGA_XSxx 6
Clock
Sys_CLK_24
Sys_CLK_150
24MHz
150MHz
FPGA_CPLD_Clock 3
UART3
UART3_TxD
UART3_RxD
UART3_RTS#
UART3_CTS#
TxD
RxD
RTS#
CTS#
CPLD_FPGA_UART3 3
FPGA_CTRL2
FPGA_DONE
FPGA_PROG_B
HDL Reset/M0
DONE
PROG_B
HDL_Res
CPLD_FPGA_CTRL2 3
BBB_P8
BBB_FPGA_GPIO2 5
FPGA_MISO UART3_TxD
FPGA_MOSI UART3_RxD
FPGA_MISO2 UART3_RTS#
FPGA_MISO3 UART3_CTS#
SPI_Memory
FPGA_MISO
FPGA_MOSI
FPGA_MISO2
FPGA_MISO3
PMOD.XS10_3_CSO_B
CLK_Mem
MISO
MOSI
MISO2
MISO3
CSO_B
CLK_Mem
FPGA_SPI_Mem 3, 8
Config Reset
SB1
222AMVBAR
3V3
U6
VDD RESET
MR PFO
PFI WDI
GND WDO
PAD
TPS3705-33DGN
FPGA_PROG_B
C60
100nF
GND
HDL Reset
SB3
R17
10k
HDL Reset/M0
FPGA_DONE R26 2.2k
FPGA_INIT_B R27 2.2k
FPGA_PROG_B R28 2.2k
1. - release U7 pin 72. route XS10 pin 3 (page 6 PMOD connectors) into U7 pin 38
2. - swap signal wires between U7 pin 70 and U7 pin 59
U12
EN Vdd
GND OUT
24MHz
C68
100nF
R31 33
Sys_CLK_24
U10
150MHz
C69
R32 33
Sys_CLK_150
Project: Beagle-DGX-XC6
Title: [2]-FPGA.SchDoc
Variant: [No Variations]
Engineer: Sergej Bakhmach
Revision: 1
Size: A4
Sheet: 2 of 10
Company: Those Boards
tb

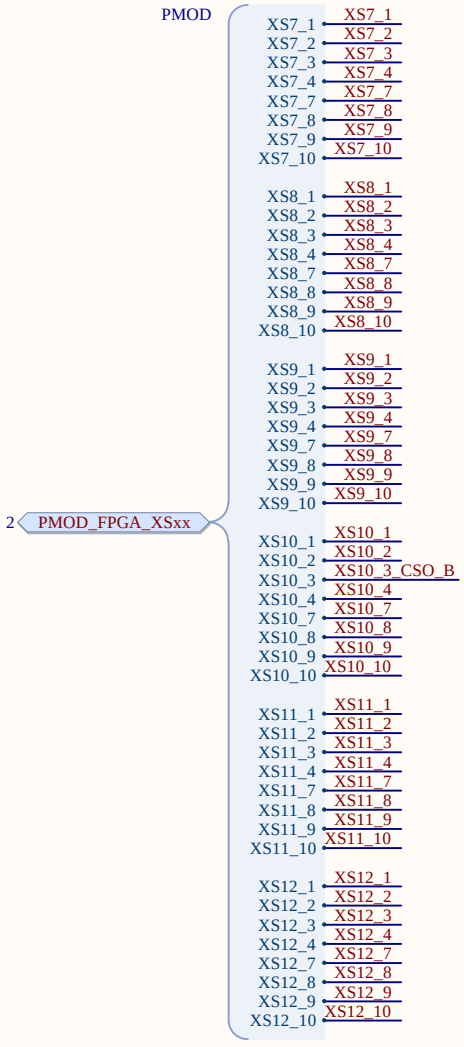

U9A
BANK 1
I/O,GCK1
Layer_Sel10
Layer_Sel9
TMS_CPLD_IO
Layer_Sel8
UART3_CTS#
UART3_RTS#
UART3_RxD
UART3_TxD
B_UART0_TX
B_UART0_RX
Sys_CLK_24
XC95144XL-10TQG100C
U9E
BANK 5
BBB_DONE
BBB_PROG_B
Layer_Sel2
Layer_Sel5
Layer_Sel1
Layer_Sel4
Layer_Sel0
Layer_Sel3
JTAG1_TDI_JP
JTAG1_TCK
XC95144XL-10TQG100C
U9I
TDI
TDO
TCK
TMS
JTAG1_TDI
JTAG1_TDO
JTAG1_TCK
JTAG1_TSM_CPLD
XC95144XL-10TQG100C
Layer Select
Layer_Sel[10..0]
BBB_CPLD_Layer_Sel
Clock
Sys_CLK_24
Sys_CLK_150
24MHz
150MHz
FPGA_CPLD_Clock
U9B
BANK 2
I/O,GSR
I/O,GTS3
I/O,GTS4
I/O,GTS1
I/O,GTS2
HDL_Reset
TP1 GTS3
TP2 GTS4
TP3 GTS2
TP4 GTS1
JTAG2_TDI
JTAG2_TCK
JTAG2_TMS
JTAG2_TDO_JP
JTAG1_TDO_JP
XC95144XL-10TQG100C
U9F
BANK 6
BCB3
BCB2
BCB1
BCB0
BDB4
BDB5
BDB6
BDB7
SUSP#
PWREN#
XC95144XL-10TQG100C
JP7
Jumper Green
J7
JTAG
IO
JTAG1_TSM_CPLD
JTAG1_TMS
TMS_CPLD_IO
TMS_sel
87224-3
B_UART0_RX
B_UART0_TX
UART0
BBB_CPLD_UART0
UART1
UART1_TxD
UART1_RxD
UART1_RTS#
UART1_CTS#
BBB_CPLD_UART1
BBB_I2C2_SCL
BBB_I2C2_SDA
SCL
SDA
BBB_I2C2
FT_BBB_I2C2
U9C
BANK 3
I/O,GCK2
I/O,GCK3
Sys_CLK_150
PMOD.XS10_3_CSO_B
CLK_Mem
CPLD_CLK
SPI1_SCLK
SPI1_DO
SPI1_DI
SPI1_CS0
Layer_Sel7
Layer_Sel6
XC95144XL-10TQG100C
U9G
BANK 7
ADB4
ADB5
ADB6
ADB7
ACB0
ACB1
ACB2
ACB3
ACB4
ACB5
XC95144XL-10TQG100C
MISO
MOSI
MISO2
MISO3
CSO_B
CLK_Mem
SPI_Memory
FPGA_SPI_Mem
PMOD.XS10_3_CSO_B
CLK_Mem
UART2_TxD
UART2_RxD
UART2_RTS#
UART2_CTS#
UART2
FT_CPLD_UART2
UART3_TxD
UART3_RxD
UART3_RTS#
UART3_CTS#
UART3
CPLD_FPGA_UART3
SPI1
SPI1_DO
SPI1_SCLK
SPI1_CS0
SPI1_DI
DO
SCLK
CS0
DI
BBB_CPLD_SPI1
Absent on PCB
JP9
JP10
JP11
J9
J10
J11
JTAG2_TDO
JTAG2_TDO_JP
JTAG1_TDO
JTAG1_TDO_JP
JTAG1_TDI
JTAG1_TDI_JP
JTAG2_TCK
JTAG2_TDI
JTAG2_TDO
JTAG2_TMS
JTAG2_FPGA
JTAG2_FPGA
CPLD_FPGA_Power_JTAG2
U9D
BANK 4
UART1_CTS#
UART1_RTS#
UART1_TxD
UART1_RxD
FPGA_DONE
FPGA_PROG_B
BBB_I2C2_SCL
BBB_I2C2_SDA
XC95144XL-10TQG100C
U9H
BANK 8
ACB6
ACB7
UART2_TxD
UART2_RxD
UART2_RTS#
UART2_CTS#
BCB7
BCB6
BCB5
BCB4
XC95144XL-10TQG100C
FT_Bus
ADB[7..4]
ACB[7..0]
BDB[7..4]
BCB[7..0]
SUSP#
PWREN#
ADB[7..4]
ACB[7..0]
BDB[7..4]
BCB[7..0]
SUSPEND#
PWREN#
FT_Ports
JTAG1_TCK
JTAG1_TDI
JTAG1_TDO
JTAG1_TMS
TCK
TDI
TDO
TMS
BUSs
FT_CPLD_FT_Ports
BBB_DONE
BBB_PROG_B
DONE
PROG_B
FPGA_CTRL1
BBB_CPLD_FPGA_CTRL1
FPGA_DONE
FPGA_PROG_B
HDL_Reset
DONE
PROG_B
HDL_Res
FPGA_CTRL2
CPLD_FPGA_CTRL2
3V3
U13
EN
Vdd
GND
OUT
3.6864MHz
C104
100nF
R33
33
CPLD_CLK
GND
3. - release U9 pin 9. apply jumper between U9 pin 9 and U7 pin 106 (page 7 - FPGA power)
4. - release U9 pin 10. apply jumper between U9 pin 10 and U9 pin 83
5. - release U9 pin 46. apply jumper between U9 pin 46 and U9 pin 45
Project: Beagle-DGX-XC6
Title: [3]-CPLD.SchDoc
Variant: [No Variations]
Engineer: Sergej Bakhmach
Revision: 1
Size: A4
Sheet: 3 of 10
Company: Those Boards
tb

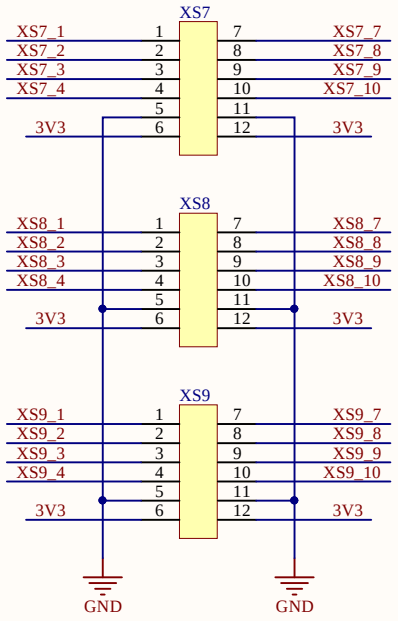


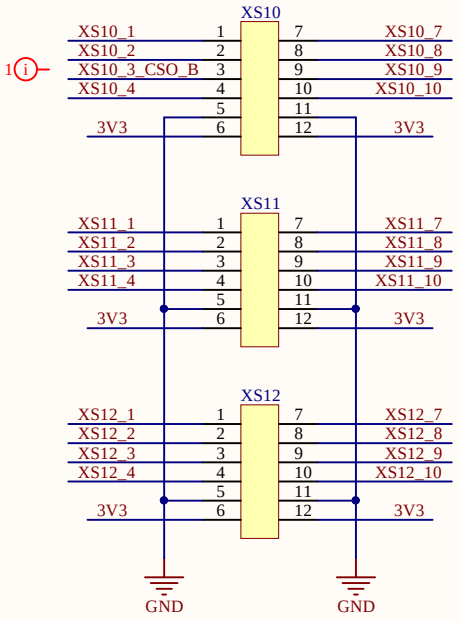
Project: **Beagle-DGX-XC6**		
Title: **[4]-USB.SchDoc**		Variant: **[No Variations]**
Engineer: Sergej Bakhmach	Revision: 1	tb
Size: A4	Sheet: 4 of 10	
Company: **Those Boards**		



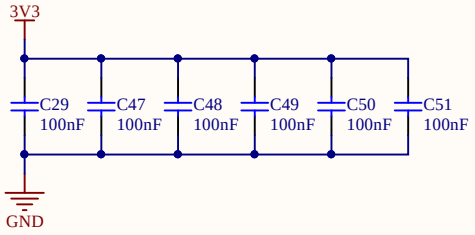
Project: **Beagle-DGX-XC6**		
Title: **[5]-BeagleBlack Connectors.SchDoc**		Variant: **[No Variations]**
Engineer: Sergej Bakhmach	Revision: 1	tb
Size: A4	Sheet: 5 of 10	
Company: **Those Boards**		



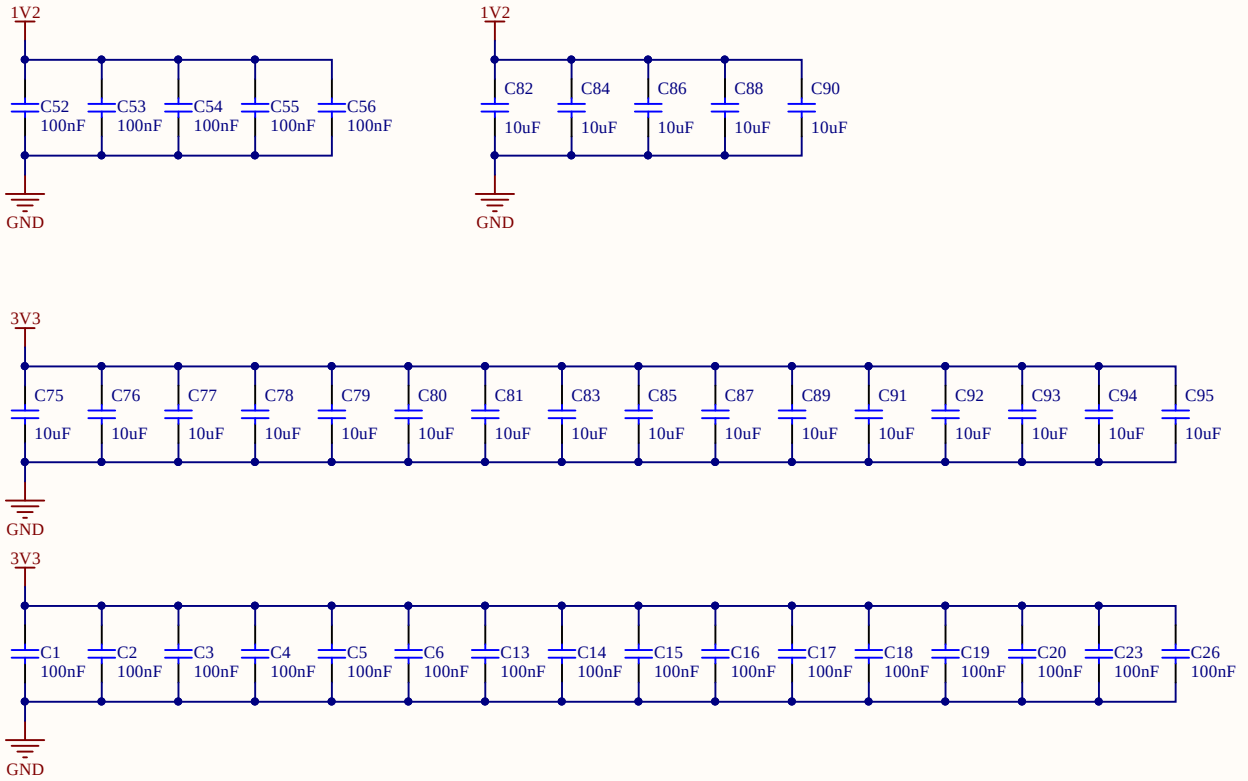


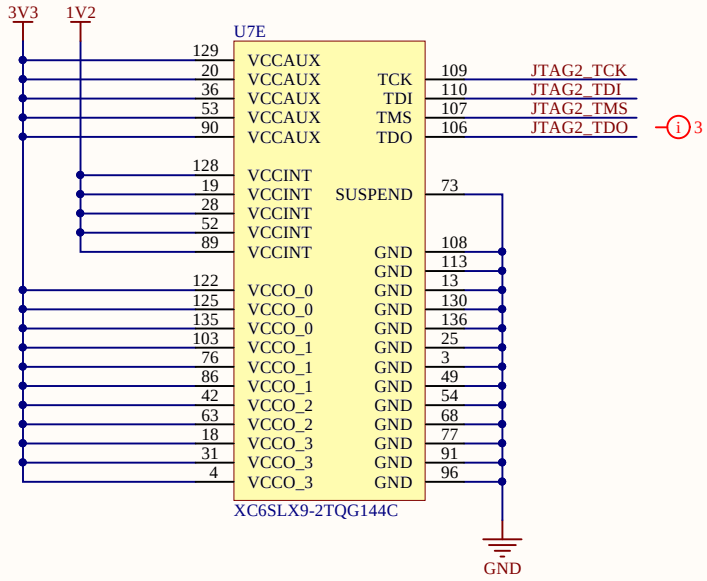


1. - see rework manual on page 2 - FPGA



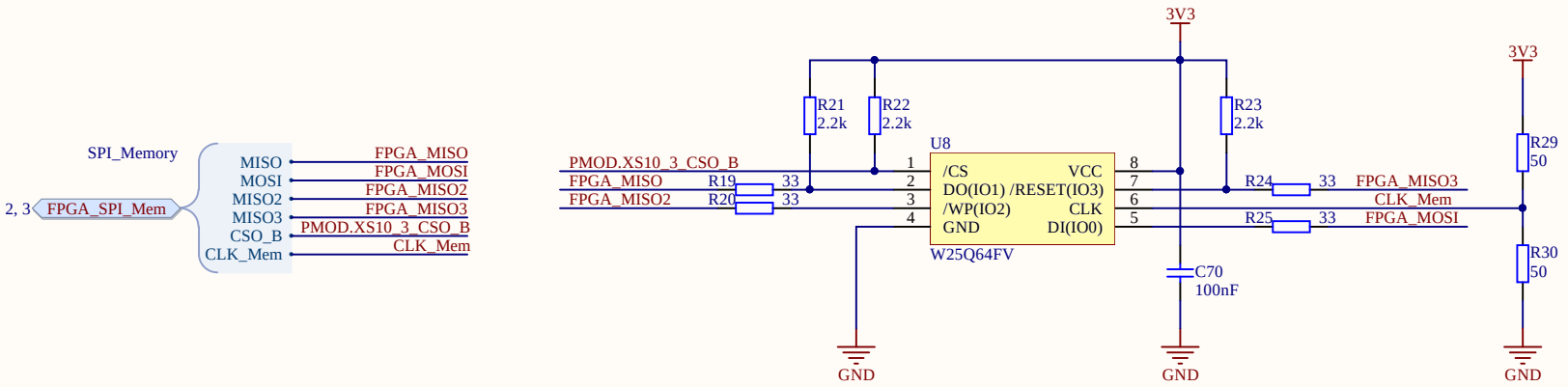
Project: **Beagle-DGX-XC6**		
Title: **[6]-PMOD Connectors.SchDoc**		Variant: **[No Variations]**
Engineer: Sergej Bakhmach	Revision: 1	tb
Size: A4	Sheet: 6 of 10	
Company: **Those Boards**		



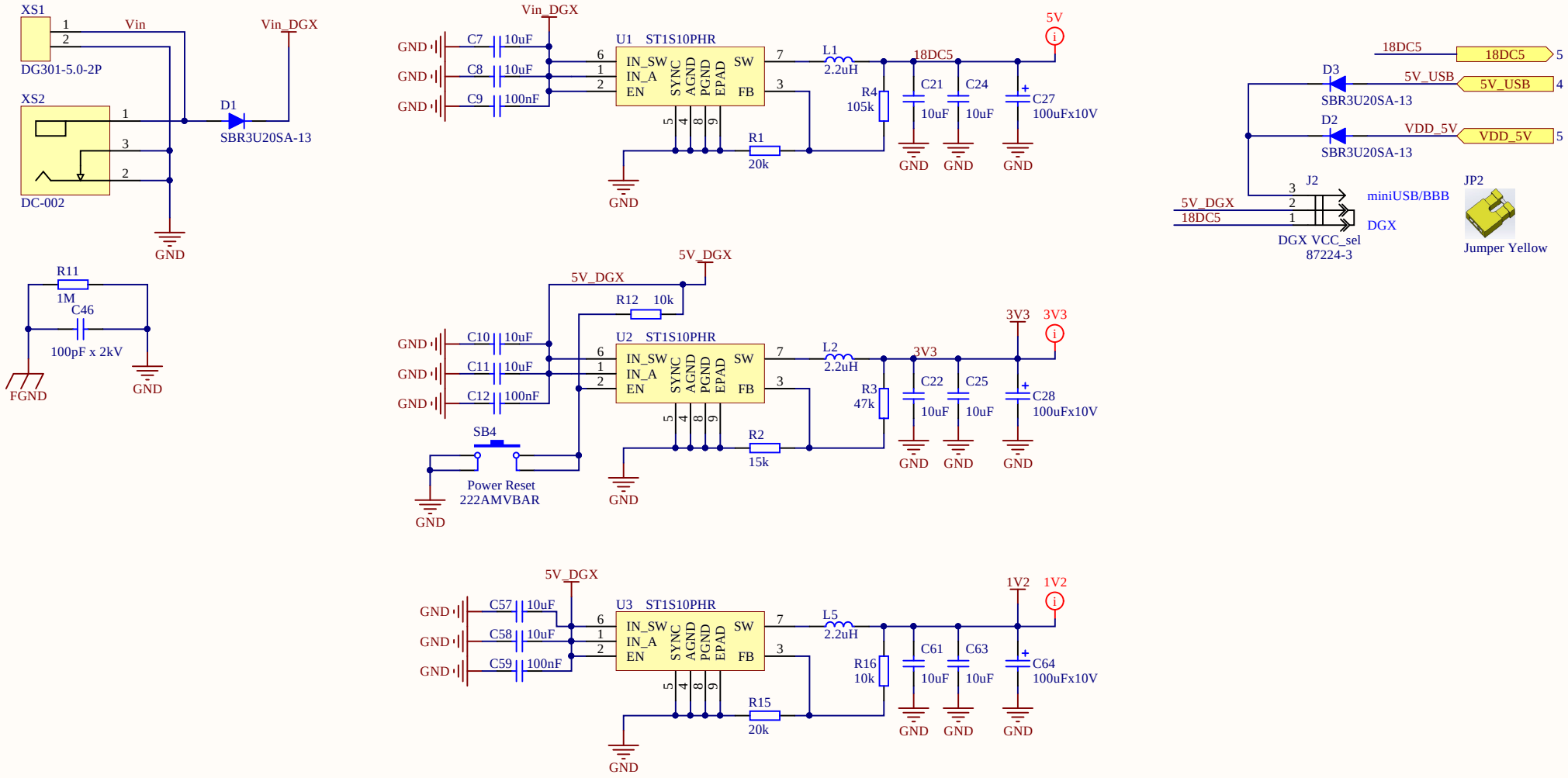


3. - see rework manual on page 2 - FPGA

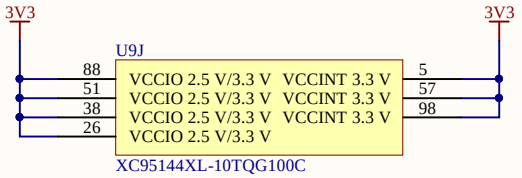
Project: **Beagle-DGX-XC6**		
Title: **[7]-FPGA-Power.SchDoc**		Variant: **[No Variations]**
Engineer: Sergej Bakhmach	Revision: 1	tb
Size: A4	Sheet: 7 of 10	
Company: **Those Boards**		

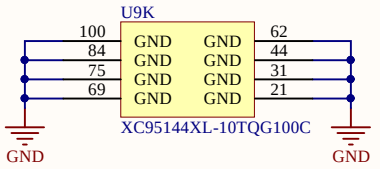


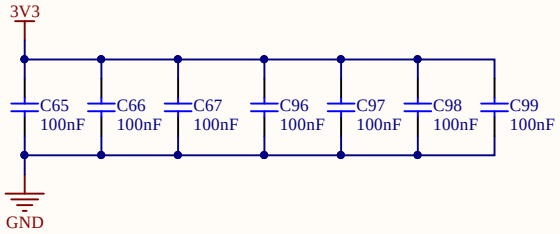
Project: **Beagle-DGX-XC6**		
Title: **[8]-SPI_Memory.SchDoc**		Variant: **[No Variations]**
Engineer: Sergej Bakhmach	Revision: 1	tb
Size: A4	Sheet: 8 of 10	
Company: **Those Boards**		

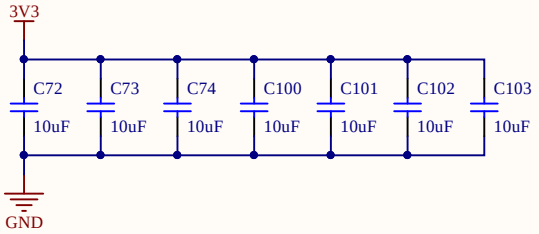


Project: **Beagle-DGX-XC6**		
Title: **[9]-Power Supply.SchDoc**		Variant: **[No Variations]**
Engineer: Sergej Bakhmach	Revision: 1	tb
Size: A4	Sheet: 9 of 10	
Company: **Those Boards**		









Project: **Beagle-DGX-XC6**		
Title: **[10]-CPLD-Power.SchDoc**		Variant: **[No Variations]**
Engineer: Sergej Bakhmach	Revision: 1	tb
Size: A4	Sheet: 10 of 10	
Company: **Those Boards**		