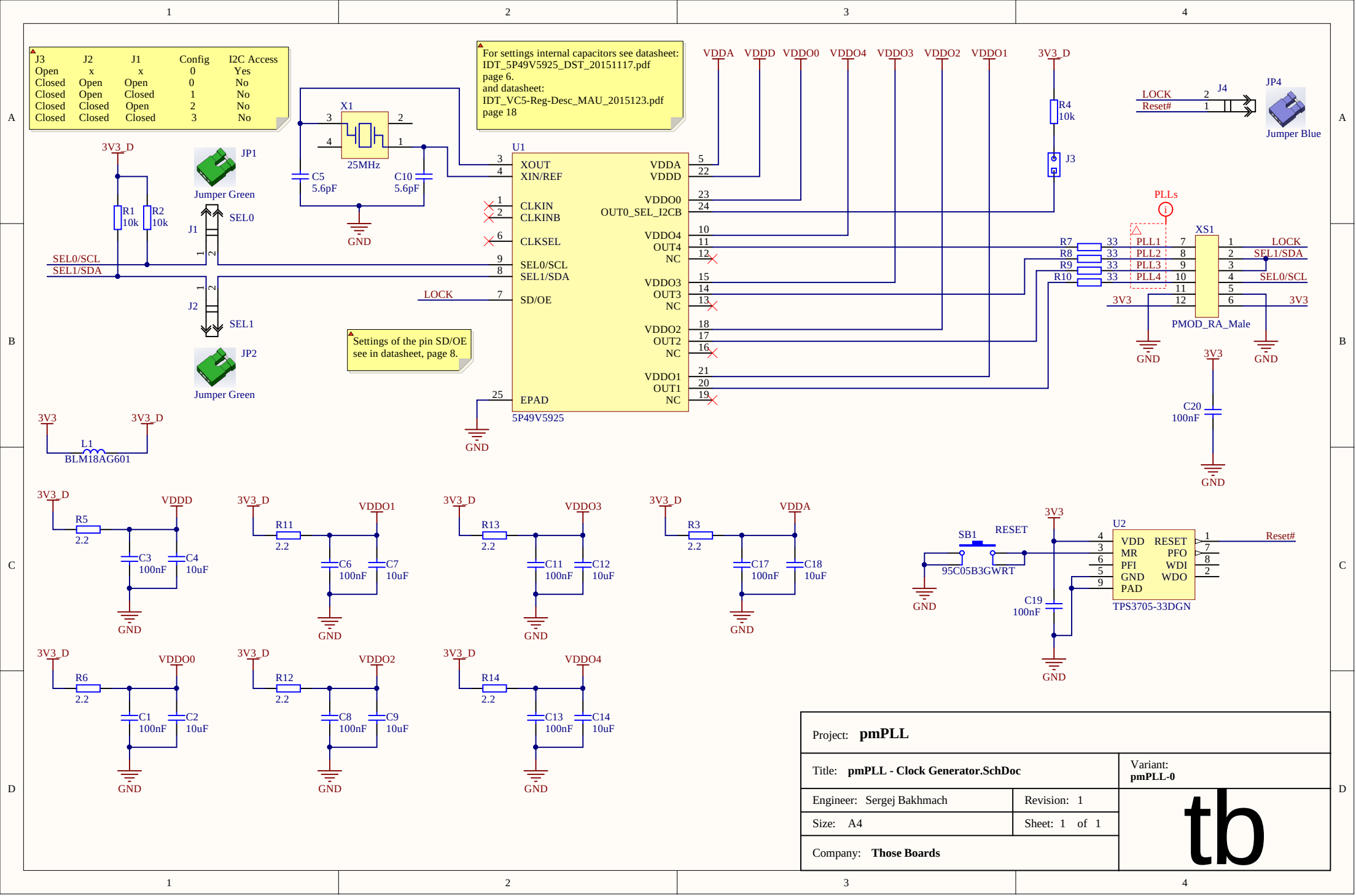
J3 J2 J1 Config I2C Access
Open x x 0 Yes
Closed Open Open 0 No
Closed Open Closed 1 No
Closed Closed Open 2 No
Closed Closed Closed 3 No
For settings internal capacitors see datasheet: IDT_5P49V5925_DST_20151117.pdf page 6. and datasheet: IDT_VC5-Reg-Desc_MAU_2015123.pdf page 18
Settings of the pin SD/OE see in datasheet, page 8.
U1
5P49V5925
XOUT
XIN/REF
CLKIN
CLKINB
CLKSEL
SEL0/SCL
SEL1/SDA
SD/OE
EPAD
VDDA
VDDD
VDDO0
OUT0_SEL_I2CB
VDDO4
OUT4
VDDO3
OUT3
VDDO2
OUT2
VDDO1
OUT1
NC
X1
25MHz
C5 5.6pF
C10 5.6pF
JP1
Jumper Green
JP2
Jumper Green
J1
J2
SEL0
SEL1
R1 10k
R2 10k
R4 10k
J3
JP4
Jumper Blue
J4
LOCK
Reset#
PLLs
XS1
PMOD_RA_Male
PLL1
PLL2
PLL3
PLL4
R7 33
R8 33
R9 33
R10 33
L1
BLM18AG601
C20 100nF
R5 2.2
R11 2.2
R13 2.2
R3 2.2
R6 2.2
R12 2.2
R14 2.2
C1 100nF
C2 10uF
C3 100nF
C4 10uF
C6 100nF
C7 10uF
C8 100nF
C9 10uF
C11 100nF
C12 10uF
C13 100nF
C14 10uF
C17 100nF
C18 10uF
SB1
RESET
95C05B3GWRT
U2
TPS3705-33DGN
VDD
MR
PFI
GND
PAD
RESET
PFO
WDI
WDO
C19 100nF
3V3_D
3V3
GND
Project: pmPLL
Title: pmPLL - Clock Generator.SchDoc
Variant: pmPLL-0
Engineer: Sergej Bakhmach
Revision: 1
Size: A4
Sheet: 1 of 1
Company: Those Boards
tb